

## **Hall A Dipole PLC Project Status**

**June 12, 2019**

*DSG Staff: Brian Eng*

1. Updated Logic on PLC for some Interlocks
  - 1.1. Jack found that some of the wiring was incorrect prior to going to the PLC
    - 1.1.1. The signals are (+) Lead Flow, (-) Lead Flow, and Quench
  - 1.2. After Jack corrected them the PLC code needed to be inverted
    - 1.2.1. Previously a Boolean 0 would indicate a good status, now it is a 1
2. Tidying up the code some
  - 2.1. After trying to verify the PLC operations found that instead of using the \*\_Status tag the code was using the input channel, made cross referencing tags much more difficult.
    - 2.1.1. Changed those so the input is only read once and thereafter the Status tag is used.